

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, the method comprising:

5 measuring a patterned gate length of a patterned gate structure;
 forming offset spacers along sides of the patterned gate structure, wherein
 a width of the offset spacers is determined according to the patterned gate
 length; and
 implanting drain extension regions of a semiconductor body after forming
10 the offset spacers.

2. The method of claim 1, wherein forming the offset spacers comprises:

 conformally depositing an offset spacer material layer over the top and
15 sides of the patterned gate structure and above prospective source/drain regions
 of the semiconductor body; and
 performing an anisotropic etch process that removes portions of the offset
 spacer material from prospective drain extension regions of the semiconductor
 body and leaves offset spacer material along the sides of the patterned gate
20 structure.

3. The method of claim 2, wherein the offset spacer material comprises silicon nitride or silicon oxide.

25 4. The method of claim 2, wherein the offset spacer material
 comprises silicon nitride, further comprising forming an oxide over the patterned
 gate structure and over the prospective drain extension regions of the
 semiconductor body prior to conformally depositing the offset spacer material
 layer.

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5. The method of claim 2, wherein the offset spacer material layer is deposited to a thickness determined according to the patterned gate length.

6. The method of claim 5, wherein the thickness of the deposited spacer material is about half the difference between a constant and the measured patterned gate length.

7. The method of claim 6, wherein the constant is related to a desired channel length.

8. The method of claim 5, wherein the anisotropic etch process is controlled according to the measured patterned gate length.

9. The method of claim 8, wherein the thickness of the deposited spacer material and the anisotropic etch process are controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

10. The method of claim 9, wherein the constant is related to a desired channel length.

11. The method of claim 2, wherein the anisotropic etch process is controlled according to the measured patterned gate length.

12. The method of claim 11, wherein the anisotropic etch process is controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

13. The method of claim 12, wherein the constant is related to a desired channel length.

14. The method of claim 2, wherein the thickness of the deposited spacer material and the anisotropic etch process are controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

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15. The method of claim 14, wherein the constant is related to a desired channel length.

16. The method of claim 1, wherein the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

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17. The method of claim 16, wherein the constant is related to a desired channel length.

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18. The method of claim 1, wherein the offset spacers comprise silicon nitride or silicon oxide.

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19. The method of claim 1, wherein measuring the patterned gate length comprises one of scanning electron microscopy, atomic force microscopy, and scatterometry.

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20. The method of claim 1, wherein measuring the patterned gate length comprises measuring a dimension of a patterned test structure in a scribe line region of a wafer.

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21. A method of fabricating a transistor, the method comprising:
forming a gate dielectric layer above a semiconductor body;
forming a gate electrode layer above the gate dielectric layer;
selectively etching the gate electrode layer to form a patterned gate structure having a patterned gate length;

measuring the patterned gate length;
determining an offset distance based on the measured patterned gate length;
forming offset spacers along laterally opposite sides of the patterned gate structure, the offset spacers extending laterally outwardly from the patterned gate structure by the offset distance; and
performing a drain extension implant with the offset spacers along the laterally opposite sides of the patterned gate structure to provide dopants to drain extension portions of the semiconductor body.

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22. The method of claim 21, wherein the offset distance is about half the difference between a constant and the measured patterned gate length.

23. The method of claim 22, wherein the constant is related to a desired channel length.

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24. A method of fabricating a semiconductor device, the method comprising:

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forming a gate dielectric layer above a semiconductor body;
forming a gate electrode layer above the gate dielectric layer;
selectively etching the gate electrode layer to form a patterned gate structure having a patterned gate length;
measuring a patterned gate length;
forming offset spacers along sides of a patterned gate structure, wherein a width of the offset spacers is determined according to the patterned gate length;
and
implanting drain extension regions of a semiconductor body after forming the offset spacers.

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25. The method of claim 24, wherein the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

5 26. The method of claim 25, wherein the constant is related to a desired channel length.